Koushal Kumar Reddy Chagari

Indian Institute of Technology Madras

Email: ee20b023@smail.iitm.ac.in

Education

Program	Institution	%/CGPA	Year of completion
B.Tech (Honors) **Electrical Engineering**	Indian Institute of Technology Madras	**9.87**	2024

Scholastic Achievements

- Ranked **1st in the Department of Electrical Engineering** among 155 students at IIT Madras
- Awarded the **Summer@EPFL** Fellowship, among a cohort of 50 students from across the world
- Awarded **Sri K Krishnamurthi Award** for the second highest CGPA in the academic year 2020-21
- Awarded **Sri V Rajagopalan Memorial Prize** for the highest CGPA in the second year of Electrical Engineering
- Awarded **B Jayant Baliga Scholarship** for the best academic record in the second year of Electrical Engineering
- Awarded **M Shankaraiah and M Sarada Scholarship** for the best academic performance in my sophomore year
- Awarded **Notional Award** for being among the top 7% of students admitted to IIT Madras on basis of JEE rank
- Nominated for **OPJEMS Scholarship** twice in 2021 and 2022 for academic and leadership excellence
- Secured All India Rank **327** out of 1,50,000 students in JEE Advanced 2020
- Secured **100 percentile** and achieved All India Rank **22** out of more than 14 lakh students in JEE Mains 2020
- Secured **4th** rank in the state out of more than 2.5 lakh students in TS EAMCET 2020
- Secured **5th** rank in the state out of more than 2.5 lakh students in AP EAMCET 2020
- Secured **International Rank 3** in NSO conducted by Science Olympiad Foundation in the year 2019-20
- Qualified for Kishore Vaigyanik Protsahan Yojana (**KVPY**) **scholarship** in both years, 2019-20 and 2018-19

Teaching Experience

- Working as a TA for course EE3110: Probability Foundations for Electrical Engineers in the Jul-Nov 2023 semester

Research Projects

- **Summer@EPFL Research Internship - Radar synchronization** — May 23 - Present

(Guide: Dr. Haitham Al Hassanieh, Sesnsing and Networking Systems - SENS Lab, EPFL)

- Synchronizing multiple AWR2243 radars to achieve coherent processing and enable a larger virtual array
- Observing **cross-talk heatmaps** between radars and stitching them to achieve higher resolution heatmaps
- Modified PCB design of AWR2243 single-chip radar to include connectors required for finer clock synchronization
- Currently on track to publish these results in the **ACM MobiCom 2024 international conference**

- **Spectrum Sensing** — Sept 22 - Present

(Bachelor's Thesis, Guide: Dr. R. David Koilpillai, Dept. of Electrical Engineering, IIT Madras)

- Implemented traditional band hopping spectrum sensing using energy-based detection on a USRP B210
- Periodically **ramping** the Local Oscillator's **center frequency** to scan the spectrum and collect data at a high rate
- Scanning the spectrum with variable bandwidth inorder to gain more insights on regions with more activity

- **Automatic RF Circuit Synthesis** — Aug 22 - May 23

(Guide: Dr. S. Aniruddhan, Dept. of Electrical Engineering, IIT Madras)

- Automated RF circuit design process which significantly reduces the design time of **RF front-ends** like LNAs, Mixers
- Used **Gradient Descent Algorithm** to achieve the minimum of a custom loss function based on specifications
- Optimized the design of **Capacitor Cross Coupled CG LNA in TSMC 65nm** process using Cadence Virtuoso

- **Design of Low Voltage Subsystem Module - Formula SAE** — May 21 - Feb 22

(Guide: Dr. Satyanarayanan Seshadri, Dept. of Applied Mechanics, IIT Madras)

- **PCB Design for Electric Car**
  - Created the **Brake System Plausibility Device** PCB as part of the shutdown circuit for detecting faulty brake pedal

- Designed the **HV check PCB** to check if the voltage in the battery pack has exceeded 60V to indicate HV status
- Simulated and tested the functioning of the fabricated PCBs to ensure proper functioning and efficient results

- 3D Harness for Electric Car
  - Developed the **entire car 2D harness** which involved interconnections across multiple system modules
  - Analyzed placement of various components so that routing is efficient, cost-effective and follows clearance rules
  - Routed wires through anchored conduits for protection, added **redundancy wiring** for robust failure management

Professional Experience

- Embedded Software Developer - Curneu MedTech Pvt Ltd — Dec 21 - Jan 22
  - Designed an accurate **real-life training system** for neurosurgeons for performing brain aneurysm operations
  - Developed code for **firmware update** and shifting firmware from **USART to USB OTG FS** communication protocol
  - Tested and debugged my code with **actual hardware interfaced with software** and documented the results

Courses Completed

- Adaptive Signal Processing
- Multirate DSP
- Probability Foundations
- Analog IC Design
- Digital Communication Systems
- Communication Networks
- Analog Circuits
- Computer Organization
- Wireless Communication
- Digital Signal Processing
- RF Integrated Circuits
- Microprocessor Theory and Lab

Course Projects

- Block Adaptive Filters (*EE6110: Adaptive Signal Processing*) — Jul 23 - Nov 23
  - Implemented efficient **block convolution** as basis for an equivalent LMS algorithm using DFT Block Adaptive Filters
  - Demonstrated computational efficiency by simulating the ϵ-NLMS algorithm for the case of **echo cancellation**
- Sequence Estimation (*EE4140: Digital Communication Systems*) — Jul 23 - Nov 23
  - Implemented the Viterbi decoder and low complexity Viterbi algorithms like the **DDFSE and M-algorithms**
  - Investigated sequential decoding using the **Stack and Fano algorithms** in comparision to the Viterbi algorithm
- MAC & TCP Interplay (*EE5150: Communication Networks*) — Jan 23 - May 23
  - Simulated the interplay between **MAC layer** and a caricature TCP like **transport layer** for various service policies
  - Compared Processor sharing, Water-filling and Max-weight scheduling on throughput and server utilization
- Synchronization and Channel Estimation for OFDM (*EE5141: Wireless Communication*) — Jan 23 - May 23
  - Simulated the CP correlation and **Schmidl-Cox** frequency offset synchronization algorithms for OFDM
  - Simulated the Zero Forcing, modified LS and FFT-based Channel Estimation algorithms for OFDM
- Circuit Blocks in an RF Transceiver (*EE6320: RF Integrated Circuits*) — Jan 23 - May 23
  - Designed a **CS LNA** with 30 dB Gain, 1.6 dB NF & a **Gilbert-cell Mixer, PA** at 3.5 GHz in TSMC 180nm process
  - Designed a VCO with **course + fine tuning** from 6.8 GHz to 7.2 GHz with a 400 MHz tuning range

Positions of Responsibility

- Low Voltage Subsystem Engineer - Raftar Formula Racing — May 21- Feb 22
  - Responsible for designing the **shutdown and safety circuits** for proper performance of the electric car
  - Contributed to various design decisions for designing **PCBs** and developing **3D harness** for the electric car
  - Competed as a team of 50 in Formula Bharat'21 and placed **1st** in the Design Event, winners of the Best Powertrain Award, and judged the **Overall Winners** of Formula Bharat'21

Volunteering & Extra-curricular activities

- Advised 20 students over 3 years in academic matters and co-curricular activities as a **Saathi Mentor**
- Coached 6 students over 2 years in academic distress as an **Acad Buddy Mentor**
- Selected for National Sports Organization (NSO) in **Shotput** and underwent Athletics training for 6 months
- Authored lucid articles based on finance concepts for the institute financial magazine InvestmentEtc